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Annealing temperature effects on the electrical characteristics of p-channel polysilicon thin film transistors

M. Cuscunà *, G. Stracci, A. Bonfiglietti, A. di Gaspare, L. Maiolo, A. Pecora, L. Mariucci, G. Fortunato

IFN-CNR, Via Cineto Romano 42, 00156 Rome, Italy

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Abstract

In this work, we studied the effects of different thermal annealing on the electrical characteristics of non-self-aligned low-temperature p-channel polycrystalline silicon (polysilicon) thin film transistors. Different thermal treatments were performed after Al-gate formation at different temperature (200 °C, 250 °C, 350 °C and 450 °C) and annealing times. We found that optimal conditions were obtained at 350 °C, with transfer characteristics showing a subthreshold slope of 0.5 V/dec, field effect mobility >100 cm^2/Vs and threshold voltage around −3.5 V. Hot carrier induced degradation was also analyzed performing bias-stress measurements on devices annealed at 350 °C and at different bias stress conditions. The experimental data show that a maximum transconductance degradation is obtained for $V_g(\text{stress}) - V_t = -4$ V while bias-stress at $V_g = V_t$ and $|V_g(\text{stress})| \gg |V_{ds}(\text{stress})|$ did not produce appreciable changes in both transfer and output characteristics.
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1. Introduction

The introduction of excimer laser crystallization in polycrystalline silicon (polysilicon) thin film transistors (TFTs) technology has produced a considerable improvement of the device performance. Indeed, achievement of field effect mobility in excess to 100 cm^2/Vs [1] has opened the doors to a number of circuit application of polysilicon TFTs. In particular, full integration of driving circuitry in active matrix liquid crystal displays (AMLCDs) [2] as well as in active matrix organic light emitting displays (AMOLEDs) [3] are, at present, the applications most actively investigated, and, thanks to the improved performance, system-on-glass could be eventually fabricated. In particular p-channel polycrystalline thin film transistors are currently used in CMOS peripheral circuitry for AMOLED as driving transistors of the organic light emitting diode (OLED).

However, conventional self-aligned polysilicon TFTs present several undesired effects in the electrical characteristics, including large off-current [4], kink effect [5] and hot carrier instabilities [6]. The kink effect increases, in digital circuits, the power dissipation and slightly degrades the switching characteristics, while, in analogue circuit applications, it reduces the maximum attainable gain as well as the common mode rejection ratio. The usual approach to reduce this effect is to limit the impact ionization contribution decreasing the electric field at the drain junction.

Degradation of the electrical characteristics related to hot carrier effects (HCE) is, of course, an important issue in polysilicon TFT circuit application. These effects are induced by the presence of intense electric fields at the drain junction, determined mainly by the abruptness of the lateral doping profile. Extensive investigation of HCE

* Corresponding author. Tel.: +39 6 41522244; fax: +39 6 41522220.
E-mail address: massimo.cuscuna@ifn.cnr.it (M. Cuscunà).

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in polysilicon TFTs has shown that, similarly to c-Si MOSFETs, the device degradation is controlled by the formation of interface states and oxide traps and charge injection in the gate oxide [7,8]. Recently, it has been also proposed that hot carrier induced defects could be generated at the grain boundaries creating a damage region close to the drain junction [8].

In this work, we analyze the electrical characteristics of non-self-aligned-TFTs fabricated according to a process we recently proposed [9], where source and drain contacts have been realized by deposition and lift-off of doped layers, thus allowing to eliminate ion-implantation. The gradual doping profile, resulting from the adopted contact formation process and further smeared by the laser annealing, enables a drain field reduction, if compared to doping profiles that can be achieved by conventional techniques. This allows a substantial reduction of the 'field enhanced' mechanisms, affecting the electrical characteristics of polysilicon TFTs at high source/drain voltages, such as kink effect and leakage current. In particular, we studied the effects of different thermal treatments, performed after Al-gate formation, at different temperatures and annealing times. We have also investigated hot carrier effects on devices annealed in N_2 at temperature 350 °C and at different bias-stress conditions.

2. Experimental

The devices were fabricated on oxidized silicon wafers, where first 100 nm thick amorphous silicon layer was deposited by PECVD and, after dehydrogenation, was irradiated by excimer laser at RT with a laser energy density about 450 mJ/cm^2. On the polysilicon surface, a sacrificial silicon dioxide layer, 100 nm thick, was deposited at RT by ECR-PECVD. The oxide thickness was chosen to obtain the same reflectivity in the capped and uncapped region ($R = 64\%$), allowing a constant melt depth of polysilicon layer during laser annealing. Then, source and drain regions have been defined by photolithography and the sacrificial oxide is etched off from these regions. In order to allow the lift-off process of the doped layer by wet etch, the oxide layer is deeply over-etched in horizontal direction (about 1 μm) [9]. The source and drain contacts are formed by plasma-doping technique [9]: the sample was first exposed to B_2H_6 plasma and then a second pass laser irradiation was performed at RT with a laser energy density 300 mJ/cm^2. At this energy density the polysilicon layer is partially melted both in the uncapped and capped regions. The dopant atoms diffuse in the molten polysilicon uncapped regions, generating a p$^+$ doped layer. After definition of the active layer island, the gate oxide is deposited (100 nm thick) at RT by ECR-PECVD. Finally, contact holes are formed and metal contacts (Al + 1% Si), for source, drain and gate electrodes, are deposited and defined. Different post-annealing treatments in N_2 have been studied at different temperatures (200 °C, 250 °C, 350 °C and 450 °C) and annealing times.

3. Analysis of electrical characteristics

Electrical measurements were performed on devices with $W = L = 20$ μm and in Fig. 1 the experimental transfer characteristics, measured at $V_{ds} = -0.1$ V, after 30 min annealing in N_2 at different temperatures (200 °C, 250 °C, 350 °C and 450 °C), are shown. As can be seen an appreciable variation of TFT electrical parameters is present. It is possible to note that by increasing annealing temperature the threshold voltage strongly decreases. In particular, a substantial change is present between devices annealed at 200 °C and 350 °C while minor variations occur at higher temperatures. Furthermore, subthreshold slope and field effect mobility are improved, increasing annealing temperature. A systematic analysis of the device parameters, field effect mobility (μ) (see Fig. 2(a)), threshold voltage (V_t) (see Fig. 2(b)) and subthreshold slope (S) (see Fig. 2(c)) is reported for increasing annealing times. As can be noted, for the low annealing temperatures (200 °C and 250 °C), the increasing annealing time produces a general improvement of all device parameters. Annealing at 350 °C produces, instead, lowest $|V_t|$ and S values, while little variation of the parameters is observed for different annealing times at this temperature. Finally, at 450 °C increasing annealing time tends to worsen the device parameters.

Similar effects, induced by thermal treatments with different annealing temperatures and times and in different gas ambient (N_2 and forming gas: $N_2 + 5\%$ H_2) have been observed in MOS capacitors using ECR-oxide as gate dielectric [10]. On the basis of the present study and of the data reported in [10], we conclude that the hydrogen passivation mechanism in the p-channel TFTs is driven by the thermal release of H-containing species present in the ECR-oxide film in combination with the catalytic action of the Al–SiO_2 interface. In particular, we propose that OH and H_2O species can be dissociated by the catalytic properties of di-aluminum oxide clusters and aluminum–silicon–oxygen clusters (zeolites), present at the

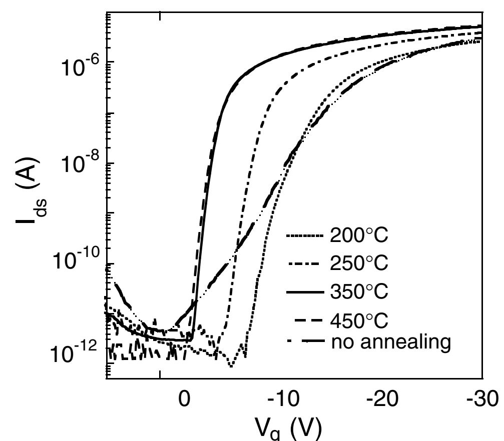

Fig. 1. TFTs transfer characteristics of p-channel TFTs, with $L = W = 20$ μm, for different annealing temperatures, measured at $V_{ds} = -0.1$ V.

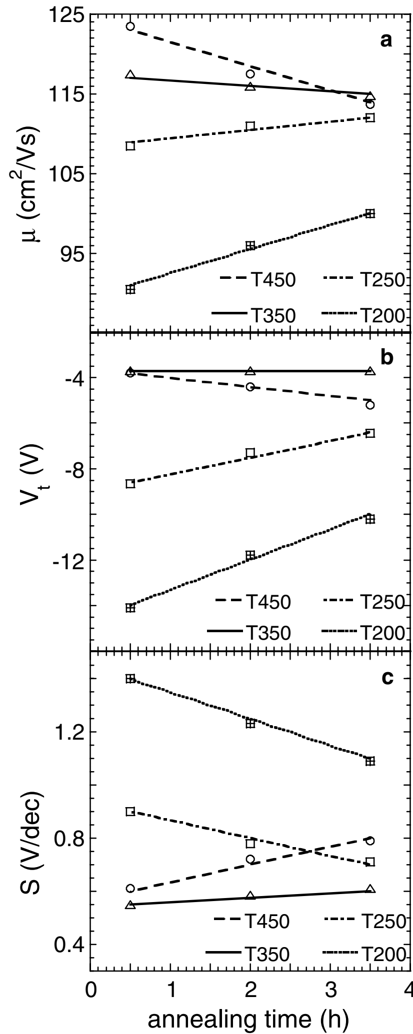

Fig. 2. (a) Field effect mobility μ, (b) threshold voltage V_t and (c) subthreshold slope S vs annealing time at different annealing temperatures: experimental data (symbols) and related linear fits (lines).

$Al–SiO_2$ interface, providing atomic hydrogen which can diffuse and passivate Si-dangling bonds at the semiconductor–insulator interface. Improvement in device parameters for increasing annealing temperature and time, in the low-temperature regime, is a consequence of enhanced release and diffusion of H-related species. However, as the temperature is increased, some Si–H bond breaking can take place at the interface, counterbalancing the effects of increased release and diffusion of H-related species. Considering the Si–H bond strength [11], it would be surprising to observe such an effect at temperatures as low as 350–450 °C. However, in the presence of a large density of Si–H bonds and/or of hydrogen atoms, as in the case of the present devices, Si–H bond breaking can also occur via the reactions [12]: $2Si–H \rightarrow 2D + H_2$; $Si–H + H \rightarrow D + H_2$, where D stands for dangling bond. As a result of the energy gained in forming an H_2 molecule, a substantial reduction of the energy required to break an isolated Si–H bond occurs. Therefore, even at low temperatures hydrogen atoms can interact with

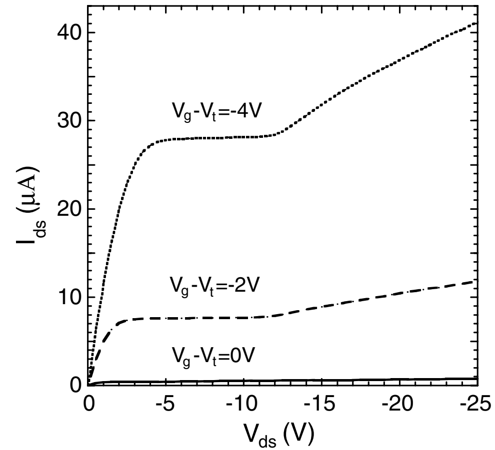

Fig. 3. Output characteristics, measured at different $V_g - V_t$, of p-channel TFTs, with $L = W = 20$ μm and annealed for 30 min at 350 °C.

dangling bonds or sub-oxide bonds at interface, resulting in a competitive Si–H depassivation mechanism.

Output characteristics are shown in Fig. 3. The good linearity observed for low V_{ds} confirms the optimal quality of the p^+ ohmic contact. The current increase observed at high drain voltage (kink effect) appears rather moderate if compared to conventional polysilicon TFTs. This result can be related to the gradual doping profile characteristic of our source/drain contact formation process. In fact the over-etch of sacrificial oxide implies the dopant gradual profile formation during the boron deposition process, further smeared by laser activation.

4. Electrical stability

The electrical stability p-channel TFTs was tested by applying prolonged bias-stress at different $V_g(\text{stress}) - V_t = 0$ V, -2 V, -4 V, -6 V, -8 V, -14 V, -20 V with $V_{ds}(\text{stress}) = -14$ V. Both transfer (measured at $V_{ds} = -0.1$ V) and output characteristics were measured before and at selected times during the bias-stressing cycle. In Fig. 4(a), are shown the transfer characteristics measured in a p-channel TFT before and for different times during bias-stress performed at $V_g(\text{stress}) - V_t = -4$ V and $V_{ds} = -14$ V. As can be seen an appreciable transconductance degradation occurs due to hot carrier effects and has been attributed to the formation of interface states at semiconductor–insulator interface close to the drain junction where the electric field is maximum [7]. Let us now discuss the behavior of the output characteristics of p-channel TFT after bias-stressing. By referring to Fig. 4(b), the I_{ds} reduction observed, at lower V_{ds}, can be explained considering that the damaged region, related to the presence of interface states, acts as a parasitic resistance in series with the undamaged channel region. At high V_{ds} (kink effect regime) the output characteristics are almost unaffected by bias-stress.

The effects of bias-stress for p-channel TFT are summarized in Fig. 5, illustrating the relative on-current reduction

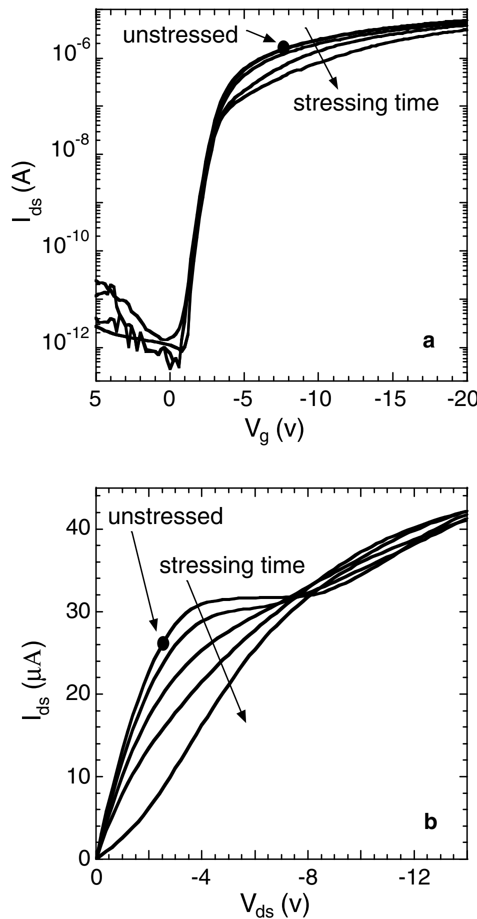

Fig. 4. (a) Transfer characteristics measured at low V_{ds} (−0.1 V) and (b) output characteristics measured at $V_g - V_t = -4$ V for p-channel TFT before bias-stress and after different stressing times (0–10 000 s). Bias-stress conditions: V_g(stress) − V_t = −4 V and V_{ds}(stress) = −14 V.

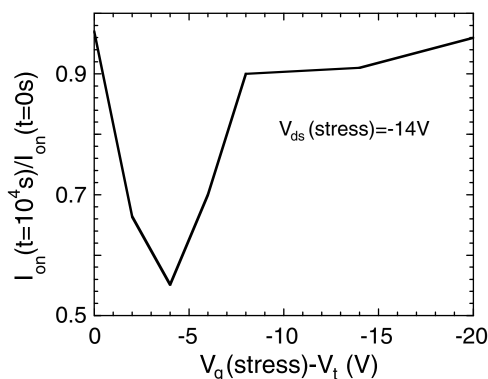

Fig. 5. $I_{on}(t = 10^4$ s$)/I_{on}(t = 0$ s$)$ ratio at different V_g(stress) − V_t with V_{ds}(stress) = −14 V, where $I_{on}(t = 10000$ s$)$ is the drain current measured after 10 000 s of bias-stress measured at $V_g = -15$ V and low V_{ds} (−0.1 V), and $I_{on}(t = 0$ s$)$ is the value measured before bias-stress at the same V_g and V_{ds}.

at different V_g(stress) − V_t and V_{ds}(stress) = −14 V. In particular, we have considered the $I_{on}(t = 10000$ s$)/I_{on}(t = 0$ s$)$ ratio, where $I_{on}(t = 10000$ s$)$ is the drain current measured after 10 000 s of bias-stress at $V_g = -15$ V and low V_{ds} (−0.1 V) and $I_{on}(t = 0$ s$)$ is the value measured before bias-stressing at the same V_g and V_{ds}. We can observe that $I_{on}(t = 10000$ s$)/I_{on}(t = 0$ s$)$ ratio decreases rapidly for lower V_g(stress) − V_t and a minimum is evident at −4 V. The maximum in device degradation occurs when combined hot-holes and hot-electrons injection is maximum, resulting in a maximum in the interface states generation rate. In fact, there is clear evidence suggesting that interface state formation is related to the sequential trapping of holes followed by electron capture (two-step model) [13]. In c-Si MOSFETs, enhanced device degradation has been experimentally observed when combined hot electron and hole emission is triggered [14]. It is interesting to note that maximum degradation in n-channel TFTs occurs at V_g(stress) = V_t [15]. The different V_g(stress) − V_t for maximum degradation found in n- and p-channel devices could be related to the different distribution of hot-hole and electron current injection and further investigation using numerical simulations is in progress. For $|V_g(\text{stress})| \gg |V_{ds}(\text{stress})|$ the transconductance degradation is reduced, as the channel becomes more accumulated and the channel potential is more uniformly distributed (linear regime), thus reducing the electric field at drain junction.

5. Conclusions

Electrical characteristics of non-self-aligned p-channel TFTs, fabricated by using plasma-doping technique for source/drain contact formation, show high field effect mobility and low threshold voltage and subthreshold slope. In addition, the kink effect in the output characteristics at high V_{ds} appears rather moderate, if compared to self-aligned polysilicon TFTs, probably due to the gradual doping profile induced by process fabrication, resulting in a reduction of electric field at the drain junction. Different post-annealing treatments were also performed, illustrating that the optimal parameters are $T = 350$ °C for $t = 30$ min, as a result of H-passivation of Si-dangling bonds at the interface. It can be noted that good electrical characteristics can be achieved even for prolonged 200 °C annealing while prolonged annealing at 450 °C tends to worsen the device parameters presumably due to breaking of Si–H bonds at the semiconductor–insulator interface. Then, the devices stability was analyzed and the electrical characteristics measured at different V_g(stress) − V_t and V_{ds}(stress) = −14 V show that a maximum transconductance degradation is obtained for V_g(stress) − V_t = −4 V while for $V_g = V_t$ and $|V_g(\text{stress})| \gg |V_{ds}(\text{stress})|$ both transfer and output characteristics remains almost unaffected.

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